19. The method of claim 17 wherein the gate electrode comprises a material selected from the group consisting of platinum, a conductive metal oxide, and ruthenium oxide.

REMARKS

Applicants respectfully request reconsideration of the subject application in light of the following Remarks and above requested Amendment.

Claim Rejections Under 35 USC §102(e)

The Examiner has rejected claims 1-6, 8-16 under 35 USC §102(e) as being anticipated by Rodder (U.S. Pat. No. 6,063,677). Claim 1 recites, "depositing a metal layer over the substrate and the alignment component". Rodder discloses that the raised source/drain regions 106 may comprise salicide, but Rodder does not disclose depositing a metal over an alignment component. In addition, claim 1 has been amended to recite, "the silicide regions having inner surfaces which face one another, wherein an upper portion of each inner surface contacts the alignment component". Rodder discloses raised source/drain regions 106 which may comprise salicide. However, the raised source/drain regions 106 which may comprise salicide do not have inner surfaces wherein an upper portion of each inner surface contacts an alignment component. Claim 1 has also been amended to recite, "a lower portion of each inner surface contacts *the semiconductor material of the substrate*". Rodder discloses a lower portion of the inner surfaces of the raised source/drain regions 106 which may comprise salicide, contacting

an insulator 114, rather than *a semiconductor material of the substrate*. Claims 2-6 and 8-16 each depend from claim 1. As a result, the Applicant respectfully requests withdrawal of the rejections of claims 1-6 and 8-16 under 35 USC §102(e).

Claim 9 recites that, "the silicide regions have lower surfaces located lower than a lower surface of the alignment component". Rodder does not disclose a silicide region having a lower surface which is lower than a lower surface of an alignment component. For this additional reason, the Applicant respectfully requests withdrawal of the rejection of claim 9 under 35 USC §102(e).

Claim 11 has been amended to recites that, "after the etching of the alignment component, *the upper portions of the inner surfaces are exposed*". In Rodder, after the first and second materials 122 and 124 of the disposable gate 120 are removed, the inner surfaces of the raised source/drain regions 106 which may comprise salicide are not exposed, instead remaining in contact with the insulation layer 114. For this additional reason, the Applicant respectfully requests withdrawal of the rejection of claim 11 under 35 USC §102(e).

Claim Rejections Under 35 USC § 103

The Examiner has rejected claim 7 under 35 USC § 103 as being unpatentable over Rodder in view or Sekine (U.S. Pat. No. 5,937,300), and claims 17-19 under 35 USC § 103 as being unpatentable over Rodder in view or Gardner (U.S. Pat. No. 6,051,865). As discussed above in reference to the 35 USC § 102 rejections, claim 1 contains many limitations that are missing from Rodder. Sekine does not disclose or suggest the limitations missing from Rodder, nor does Gardner disclose or suggest the

limitations missing from Rodder. Since claims 7 and 17-19 depend from claim 1, the Applicant respectfully requests withdrawal of the rejections of claims 7 and 17-19 under 35 USC §103.

Conclusion

For the forgoing reasons, the Applicant submits that claims 1-19 are now in condition for allowance and indication of allowance by the Examiner is respectfully requested.

If there are any additional charges, please charge Deposit Account 02-2666. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact William W. Kidd at (512) 330-0844.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE:

1. (Amended Once) A method of forming a transistor, comprising:

forming an alignment component on a substrate of a semiconductor material;

depositing a metal layer over the substrate and the alignment component;

reacting the metal layer with the semiconductor material of the substrate to form two silicide regions, the silicide regions having inner surfaces which face one another, wherein an upper portion of each inner surface contacts the alignment component [substantially extending up to the alignment component on opposing sides of the alignment component] and a lower portion of each inner surface contacts the semiconductor material of the substrate; and

replacing the alignment component with a conductive gate [substantially extending up to the silicide regions].

9. (Amended Once) The method of claim 1 wherein the silicide regions have lower surfaces located lower than a lower surface of the alignment component[, and inner surfaces, facing one another, which are in contact with the semiconductor material of the substrate].

10. (Amended Once) The method of claim 1 wherein the alignment component is replaced with the gate according to a method comprising:

depositing a layer over the silicide regions and the alignment component;

planarizing the layer at least until the alignment component is exposed;

etching the alignment component at least until the substrate is exposed to leave an opening [in the first layer] between the inner surfaces of the silicide regions; and

[filling the opening with the gate] forming the gate in the opening.

11. (Amended Once) The method of claim 10 wherein, after the etching of the alignment component, the upper portions of the inner surfaces are exposed [the silicide regions extend substantially up to the opening].